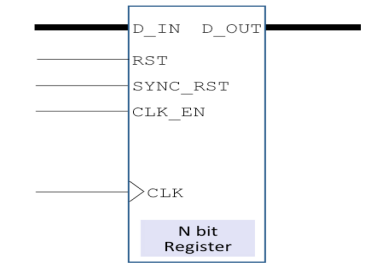
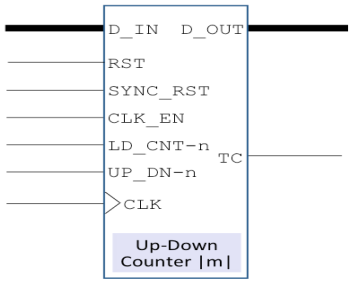
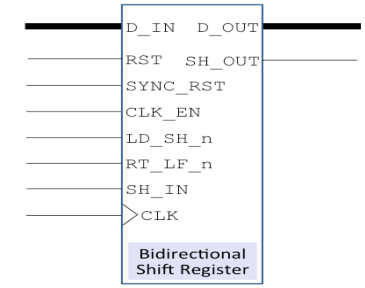
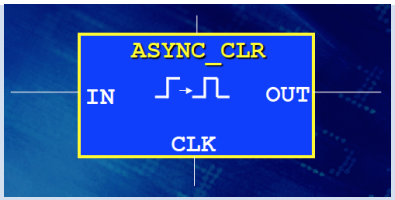
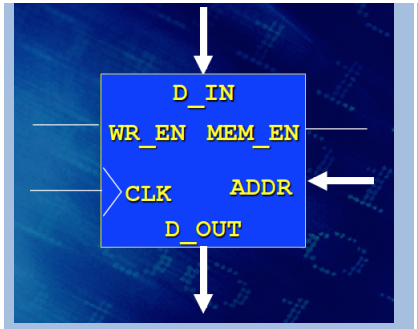
| Name | Figure | Input data | Output data | Clock | Reset | Input control | Output control |
|---|---|---|---|---|---|---|---|
| N bit Register |  | D_IN(n-1 downto 0) | D_OUT (n-1 downto 0) | CLK | RST | CLK_EN, SYNC_CLR (syn clear) | - |
| Up-down counter \|m\| |  | D_IN (n-1 downto 0) | D_OUT (n-1 downto 0) | CLK | RST | CLK_EN, SYNC_CLR, LD_CNT_n (parallel loading when asserted), UP_DN_n (count direction) | TC (terminal count). |
| Shift register |  | D_IN (n-1 downto 0), SH_IN (valore da inserire nella cella libera). | D_OUT (n-1 downto 0) | CLK | RST | CLK_EN, SYNC_RST, LD_SH_n (parallel loading when asserted, shifting otherwise), RT_LF_n (shifting direction). | SH_OUT (valore contenuto nell'ultima cella). |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pulse generator |  | IN | OUT | CLK | ASYNC_CLR | - | - |
| Single port RAM |  | D_IN (n-1 downto 0), ADDR. | D_OUT (n-1 downto 0). | CLK | - | WR_EN, MEM_EN | - |
| Dual port RAM |  | D_IN_A, D_IN_B, ADDR_A, ADDR_B. | D_OUT_A, D_OUT_B. | CLK_A, CLK_B | - | WR_EN_A, WR_EN_B. | - |